

1 CLAIMS
2
34 1. An integrated circuit comprising:
5
6 a first three-terminal device of a first type; and
7
8 a second three-terminal device of the first type, a first terminal of the second three-
9 terminal device electrically coupled to a first terminal of the first three-terminal device, and a
10 second terminal of the second three-terminal device electrically coupled to a second terminal of
11 the first three-terminal device,
12
13 wherein:14 a reference current applied to a third terminal of the second three-terminal device
15 generates a control voltage applied to the second terminals of the first and second three-terminal
16 devices;17 where the control voltage is a function of comparing an output voltage at the third
18 terminal of the second three-terminal device to a reference voltage; and
1920 the reference current is derived from the reference voltage and a reference
21 resistance.

22 2. The integrated circuit of claim 1 wherein:

23 the second three-terminal device has a different output impedance than the first three-
24 terminal device.

25 3. The integrated circuit of claim 2 wherein:

26 the second three-terminal device has a larger output impedance than the first three-
27 terminal device.

1 4. The integrated circuit of claim 1 further comprising:
2 a supply voltage electrically coupled to the first terminals of the first and second three-
3 terminal devices.

- 1 5. The integrated circuit of claim 1 wherein:
 - 2 the second terminal of the first three-terminal device is a first control terminal for the first
 - 3 three-terminal device; and
 - 4 the second terminal of the second three-terminal device is a second control terminal for the second three-terminal device;
 - 5 the second three-terminal device.

1 6. The integrated circuit of claim 1 further comprising:

2 a first resistor coupled to a third terminal of the first three-terminal device;

3 a second resistor coupled to the third terminal of the second three-terminal device; and

4 an output of the integrated circuit coupled to the first resistor,

5 wherein:

6 the reference current is applied to the third terminal of the second three-terminal

7 device through the second resistor; and

8 the output voltage at the third terminal of the second three-terminal device is

9 measured from the second resistor.

1 7. The integrated circuit of claim 6 wherein:
2 an output impedance at the output of the integrated circuit comprises an output
3 impedance of the first three-terminal device and an impedance of the first resistor.

1 8. The integrated circuit of claim 7 wherein:
2 the impedance of the first resistor is greater than the output impedance of the first three-
3 terminal device.

1 9. The integrated circuit of claim 8 wherein:
2 the output impedance of the integrated circuit is substantially linear across an operating
3 range of an output voltage at the output of the integrated circuit.

1 10. The integrated circuit of claim 1 further comprising:
2 an output of the integrated circuit coupled to a third terminal of the first three-terminal
3 device; and
4 a capacitor coupling the second terminals of the first and second three-terminal devices to
5 the output of the integrated circuit.

1 11. The integrated circuit of claim 10 wherein:
2 the capacitor controls a slew rate of an output voltage at the output of the integrated
3 circuit.

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1 12. The integrated circuit of claim 1 further comprising:

2 a third three-terminal device of the first type, a first terminal of the third three-terminal
3 device electrically coupled to the first terminals of the first and second three-terminal devices, a
4 second terminal of the third three-terminal device removably and electrically coupled to the first
5 and second terminals of the first and second three-terminal devices, and a third terminal of the
6 third three-terminal device electrically coupled to a third terminal of the first three-terminal
7 device; and

8 a fourth three-terminal device of the first type, a first terminal of the fourth three-terminal

9 device electrically coupled to the first terminals of the first, second, and third three-terminal
10 devices, a second terminal of the fourth three-terminal device removably and electrically coupled
11 to the first terminals of the first, second, and third three-terminal devices and to the second
12 terminals of the first and second three-terminal devices.

1 13. The integrated circuit of claim 1 further comprising:

2 an output of the integrated circuit coupled to a third terminal of the first three-terminal
3 device;

4 a third three-terminal device of the first type, a first terminal of the third three-terminal

5 device coupled to a third terminal of the second three-terminal device, and a third terminal of the
6 third three-terminal device coupled to the second terminals of the first and second three-terminal
7 devices;

8 an amplifier comprising two inputs and an output, a first one of the two inputs coupled to

9 the third terminal of the second three-terminal device and to the first terminal of the third three-

10 terminal device, the output coupled to a second terminal of the third three-terminal device, and a
11 second one of the two inputs coupled to the reference voltage; and
12 a current source providing the reference current and coupled to the third terminal of the
13 third three-terminal device and to the second terminals of the first and second three-terminal
14 devices.

1 14. The integrated circuit of claim 13 further comprising:
2 a first resistor coupling the output of the integrated circuit to the third terminal of the first
3 three-terminal device; and
4 a second resistor coupling the third terminal of the second three-terminal device to the
5 first one of the two inputs of the amplifier and to the first terminal of the third three-terminal
6 device,

7 wherein:
8 the reference current is applied to the third terminal of the second three-terminal
9 device through the second resistor and through the third three-terminal device; and
10 the output voltage at the third terminal of the second three-terminal device is
11 measured from the second resistor.

1 15. The integrated circuit of claim 13 further comprising:
2 a capacitor coupling the second terminals of the first and second three-terminal devices,
3 the third terminal of the third three-terminal devices, and the current source to the output of the
4 integrated circuit.

1 16. The integrated circuit of claim 15 wherein:

2 the capacitor controls a slew rate of an output voltage at the output of the integrated
3 circuit.

1 17. The integrated circuit of claim 13 further comprising:

2 a first resistor coupling the output of the integrated circuit to the third terminal of the first
3 three-terminal device;

4 a second resistor coupling the third terminal of the second three-terminal device to the
5 first one of the two inputs of the amplifier and to the first terminal of the third three-terminal
6 device; and

7 a capacitor coupling the second terminals of the first and second three-terminal devices,
8 the third terminal of the third three-terminal devices, and the current source to the output of the
9 integrated circuit and to the first resistor;

10 wherein:

11 the reference current is applied to the third terminal of the second three-terminal
12 device through the second resistor and through the third three-terminal device;

13 the output voltage at the third terminal of the second three-terminal device is
14 measured from the second resistor; and

15 the capacitor controls a slew rate of an output voltage at the output of the
16 integrated circuit.

1 18. The integrated circuit of claim 1 further comprising:

2 an output of the integrated circuit coupled to a third terminal of the first three-terminal

3 device;

4 an amplifier comprising two inputs and an output, a first one of the two inputs coupled to

5 a third terminal of the second three-terminal device, a second one of the two inputs coupled to

6 the reference voltage, and the output coupled to the second terminals of the first and second

7 three-terminal devices; and

8 a current source providing the reference current and coupled to the first one of the two

9 inputs of the amplifier and to the third terminal of the second three-terminal device.

1 19. The integrated circuit of claim 18 further comprising:

2 a first resistor coupling the output of the integrated circuit to the third terminal of the first

3 three-terminal device; and

4 a second resistor coupling the third terminal of the second three-terminal device to the

5 first one of the two inputs of the amplifier and to the current source,

6 wherein:

7 the reference current is applied to the third terminal of the second three-terminal

8 device through the second resistor; and

9 the output voltage at the third terminal of the second three-terminal device is

10 measured from the second resistor.

1 20. The integrated circuit of claim 18 further comprising:
2 a capacitor coupling the second resistor, the first one of the two inputs of the amplifier,
3 and the current source to the first resistor and to the output of the integrated circuit.

1 21. The integrated circuit of claim 20 wherein:
2 the capacitor controls a slew rate of an output voltage at the output of the integrated
3 circuit.

1 22. The integrated circuit of claim 18 further comprising:

2 a first resistor coupling the output of the integrated circuit to the third terminal of the first

3 three-terminal device;

4 a second resistor coupling the third terminal of the second three-terminal device to the

5 first one of the two inputs of the amplifier and to the current source; and

6 a capacitor coupling the second resistor, the first one of the two inputs of the amplifier,

7 and the current source to the first resistor and to the output of the integrated circuit,

8 wherein:

1 23. A driver circuit comprising:

2 a first MOSFET having a first gate electrode, a first drain electrode, and a first source

3 electrode;

4 a first resistor coupled to the first drain electrode;

5 an output of the driver circuit coupled to the first resistor;

6 a second MOSFET having a second gate electrode, a second drain electrode, and a

7 second source electrode, the first and second gate electrodes coupled together and the first and

8 second source electrodes coupled together;

9 a second resistor coupled to the second drain electrode;

10 a third MOSFET having a third gate electrode, a third drain electrode, and a third source

11 electrode, the third source electrode coupled to the second resistor;

12 an amplifier having a first amplifier input, a second amplifier input, and an amplifier

13 output, the first amplifier input coupled to the second resistor and the third source electrode, the

14 second amplifier input coupled to a reference voltage, and the amplifier output coupled to the

15 third gate electrode; and

16 a current source coupled to the third drain electrode, the first gate electrode, and the

17 second gate electrode.

1 24. The driver circuit of claim 23 wherein:

2 the second MOSFET has a larger output impedance than the first MOSFET; and

3 the second resistor has a larger impedance than the first resistor.

1 25. The driver circuit of claim 24 wherein:
2 an output impedance of the driver circuit at the output of the driver circuit comprises an
3 output impedance of the first MOSFET and an impedance of the first resistor;
4 the impedance of the first resistor is greater than the output impedance of the first
5 MOSFET such that the output impedance of the driver circuit is substantially linear.

1 26. The driver circuit of claim 25 further comprising:
2 a capacitor coupling output of the driver circuit to the third drain electrode, the first and
3 second gate electrodes, and the current source to control a slew rate of an output voltage at the
4 output of the driver circuit.

1 27. The driver circuit of claim 25 further comprising:
2 a fourth MOSFET having a fourth gate electrode, a fourth drain electrode, and a fourth
3 source electrode, the fourth drain electrode coupled to the first resistor and the first drain
4 electrode, and the fourth source electrode coupled to the first and second source electrodes; and
5 a first switch coupling the fourth gate electrode to the first and second gate electrodes and
6 the current source.

1 28. The driver circuit of claim 27 further comprising:
2 a fifth MOSFET having a fifth gate electrode, a fifth drain electrode, and a fifth source
3 electrode, the fifth drain electrode coupled to the first resistor and the first and fourth drain
4 electrodes, and the fifth source electrode coupled to the first, second, and fourth source
5 electrodes;

6 a second switch coupling the fifth gate electrode to the first and second gate electrodes
7 and the current source;
8 a third switch coupling the fifth gate electrode to the first, second, fourth and fifth source
9 electrodes; and
10 a fourth switch coupling the fourth gate electrode to the first, second, fourth, and fifth
11 source electrodes.

1 29. The driver circuit of claim 28 further comprising:
2 a capacitor coupling the output of the driver circuit and the first resistor to the first and
3 second gate electrodes, the third drain electrode, and the current source to control a slew rate of
4 an output voltage at the output of the driver circuit.

1 30. The driver circuit of claim 29 further comprising:
2 a fifth switch coupling the first and second gate electrodes, the capacitor, the third drain
3 electrode, and the current source to the first, second, fourth, and fifth source electrodes,
4 wherein:
5 the first and third switches are simultaneously opened and closed; and
6 the second and fourth switches are simultaneously opened and closed.

1 31. An integrated circuit comprising:

2 a voltage-mode driver circuit having an integral, analog on-chip termination.

1 32. The integrated circuit of claim 31 wherein:

2 the voltage-mode driver circuit has a substantially constant output impedance within an

3 operating range of an output voltage of the voltage-mode driver circuit.

1 33. A method of controlling output impedance of a driver circuit comprising:
2 generating a reference voltage as a function of a reference current and a reference
3 resistance;
4 using a first sub-circuit to generate the output impedance of the driver circuit;
5 using a second sub-circuit with a feedback loop to generate a control voltage; and
6 using the control voltage to control the output impedance.

1 34. The method of claim 33 wherein:

2 the second sub-circuit is a replica of the first sub-circuit.

1 35. The method of claim 34 wherein:

2 the second sub-circuit is a scaled replica of the first sub-circuit.

1 36. The method of claim 33 wherein:

2 using the control voltage further comprises adjusting the control voltage to keep the
3 output impedance substantially linear across an operating range of an output voltage of the driver
4 circuit.

1 37. A method of controlling output impedance of a driver circuit comprising:
2 generating a reference current as a function of a reference voltage and a reference
3 resistance;
4 using a first sub-circuit to generate the output impedance of the driver circuit;
5 using a second sub-circuit with a feedback loop to generate a control current; and
6 using the control current to control the output impedance.

1 38. The method of claim 37 wherein:
2 the second sub-circuit is a replica of the first sub-circuit.

1 39. The method of claim 38 wherein:
2 the second sub-circuit is a scaled replica of the first sub-circuit.

1 40. The method of claim 37 wherein:
2 using the control voltage further comprises adjusting the control voltage to keep the
3 output impedance substantially linear across an operating range of an output voltage of the driver
4 circuit.